

Symbols and Abbreviations

A_0	DC open loop voltage gain
A_{V_T}	Matching constant for threshold voltage
A_β	Matching constant for current factor
β	Current factor
BW	Bandwidth
C_C	Compensation capacitance
C_{GD}	Gate-drain capacitance
C_{GS}	Gate-source capacitance
C_L	Load capacitance
C_{ox}	Specific oxide capacitance
C_{par}	Parasitic capacitance
C_{th}	Thermal capacitance in self heating model
ϵ_r	Dielectric constant
E_G	Bandgap energy
ef	Exponent of flicker noise frequency dependence
F	Electric field
f	Frequency
f_{ain}	Analog input frequency
f_{chop}	Chopping frequency
f_{max}	Maximum oscillation frequency
f_{nd}	Non-dominant pole frequency
f_{sample}	Sampling frequency
f_t	Transit frequency
g_{ds}	Small signal output conductance
g_m	Small signal transconductance
h_{fin}	Fin height
I_D	Drain current
I_{B2B}	Band-to-band tunneling current
I_{GATE}	Gate current at $V_{GS} = 0, V_{DS} = V_{DD}$
I_{ON}	On current at $V_{GS} = V_{DS} = V_{DD}$
I_{OFF}	Off current at $V_{GS} = 0, V_{DS} = V_{DD}$

I_S	Diode saturation current
κ	Dielectric constant
K_f	Flicker noise coefficient
k_i	Scaling coefficient i of time constants in V_{shift} model
L_{el}	Effective channel length
L or L_{gate}	Transistor gate length
L_{min}	Minimum transistor gate length
μ	Charge carrier mobility
n	Number of bits
N	Noise power
N_A	Doping level
P	Power
$\Phi_{1/2}$	Complementary, non-overlapping clock phases
R_{DD}	Sensitivity of output current against supply voltage variations
R_G	Gate resistance
R_{Leak}	Diode leakage resistance
R_{out}	Output resistance
R_{SD}	Source-drain series resistance
R_{scale}	Scaling resistance in V_{shift} model
R_{th}	Thermal resistance in self heating model
s	Scaling factor
S	Signal power
T	Temperature
t_{dep}	Penetration depth of gate field
t_{eval}	Evaluation time
t_{ox}	Oxide thickness
t_{si}	Thickness of silicon layer
t_{stress}	Stress time
V_{bi}	Build in source potential
V_{CM}	Common mode voltage
V_{DD}	Positive supply voltage
V_D	Diode voltage
V_{DS}	Drain-source voltage
V_{GS}	Gate-source voltage
V_{ov}	Overdrive voltage $V_{GS} - V_T$
$V_{ref(p)(n)}$	(Positive) (negative) reference voltage
V_T	Threshold voltage
V_{the}	Thermal voltage
V_{shift}	Shift voltage representing time dependent V_T shift
V_{SS}	Negative supply voltage
V_{ss}	Maximum steady state V_T shift
V_{stress}	Stress voltage
w_{fin}	Fin width
W	Transistor (gate) width
x_j	Junction depth

ADC	Analog-to-digital converter
BEOL	Back end of line (metallization)
BGR	Bandgap reference
BOX	Buried oxide layer
CMRR	Common mode rejection ratio
DAC	Digital-to-analog converter
DIBL	Drain induced barrier lowering
DNL	Differential non-linearity
EI	Electrostatic integrity
ENOB	Effective number of bits
EOT	Equivalent oxide thickness
FD	Fully depleted
FET	Field effect transistor
GBW	Gain bandwidth product
INL	Integral non-linearity
IPTAT	Inverse proportional to absolute temperature
LDD	Lightly doped drain
LNA	Low noise amplifier
LSB	Least significant bit
MuGFET	Multi-gate FET
MuGTFET	Multi-gate tunneling FET
NDR	Negative differential resistance
NTF	Noise transfer function
OPC	Optical proximity correction
OSR	Oversampling ratio
PLL	Phase locked loop
PSRR	Power supply rejection ratio
SAR	Successive approximation register
SCE	Short channel effect
SEG	Selective epitaxial growth
SFDR	Spurious free dynamic range
SIP	System in package
SNDR	Signal-to-noise-and-distortion ratio
SNR	Signal-to-noise ratio
SOC	System on chip
SOI	Silicon on insulator
SR	Slew rate
(P)(N)TC	(Positive) (negative) temperature coefficient
TFET	Tunneling FET
THD	Total harmonic distortion
VCO	Voltage controlled oscillator
VIP3	Third order interception point
VTRO	Threshold voltage roll-off

References

1. T. Luftner, J. Berthold, C. Pacha, G. Georgakos, G. Sauzon, O. Homke, J. Beshenar, P. Mahrle, K. Just, P. Hober, S. Henzler, D. Schmitt-Landsiedel, A. Yakovleff, A. Klein, R. Knight, P. Acharya, H. Mabrouki, G. Juhoor, M. Sauer, A 90 nm CMOS low-power GSM/EDGE multimedia-enhanced baseband processor with 380 MHz ARM9 and mixed-signal extensions, in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, 6–9 February 2006, pp. 952–961
2. M. Hammes, C. Kranz, J. Kissing, D. Seippel, P.-H. Bonnaud, E. Pelos, A GSM baseband radio in 0.13 μm CMOS with fully integrated power-management, in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers (2007)*, pp. 264–602
3. S. Heinen, Architectures and circuit techniques for nanoscale RF CMOS, in *ISSCC Advanced Design Forum (2008)*
4. International Technology Roadmap for Semiconductors, <http://www.itrs.net>, 2007 edn. Chap. System Drivers
5. B.S. Meyerson, Opening keynote address—how does one define “technology” now that classical scaling is dead (and has been for years)? in *Proceedings of 42nd Design Automation Conference*, June 2005, p. 25
6. K. von Arnim, E. Augendre, C. Pacha, J. Berthold, T. Schulz, K.T. San, F. Bauer, A. Nackaerts, R. Rooyackers, N. Collaert, T. Vandeweyer, B. Degroote, A. Dixit, R. Siganamalla, W. Xiong, A. Marshall, C.-R. Cleavelin, K. Schrufer, M. Jurczak, A low-power multi-gate FET CMOS technology with 13.9 ps inverter delay, large-scale integrated high performance digital circuits and SRAM, in *Symposium on VLSI Technology, Digest of Technical Papers (2007)*, pp. 106–107
7. C. Pacha, K. von Arnim, F. Bauer, T. Schulz, W. Xiong, K.T. San, A. Marshall, T. Baumann, C.-R. Cleavelin, K. Schrufer, J. Berthold, Efficiency of low-power design techniques in multi-gate FET CMOS circuits, in *Proceedings of 33th European Solid-State Circuits Conference, ESSCIRC (2007)*, pp. 111–114
8. G. Knoblinger, F. Kuttner, A. Marshall, C. Russ, P. Haibach, P. Patruno, T. Schulz, W. Xiong, M. Gostkowski, K. Schrufer, C.R. Cleavelin, Design and evaluation of basic analog circuits in an emerging MuGFET technology, in *2005 IEEE International SOI Conference Proceedings (IEEE Press, New York, 2005)*, pp. 39–40
9. International Technology Roadmap for Semiconductors, <http://www.itrs.net>, 2007 edn. Chap. Process Integration, Devices, and Structures
10. R. Khamankar, H. Bu, C. Bowen, S. Chakravarthi, P.R. Chidambaram, M. Bevan, A. Krishnan, H. Niimi, B. Smith, J. Blatchford, B. Hornung, J.P. Lu, P. Nicollian, B. Kirkpatrick, D. Miles, M. Hewson, D. Farber, L. Hall, H. Alshareef, A. Varghese, A. Gurba, V. Ukraintsev, B. Rath-sack, J. DeLoach, J. Tran, C. Kaneshige, M. Somervell, S. Aur, C. Machala, T. Grider, An enhanced 90 nm high performance technology with strong performance improvements from

- stress and mobility increase through simple process changes, in *Symposium on VLSI Technology, Digest of Technical Papers*, June 2004, pp. 162–163
11. A. Steegen, R. Mo, R. Mann, M.-C. Sun, M. Eller, G. Leake, D. Vietzke, A. Tilke, F. Guarin, A. Fischer, T. Pompl, G. Massey, A. Vayshenker, W.L. Tan, A. Ebert, W. Lin, W. Gao, J. Lian, J.-P. Kim, P. Wrschka, J.-H. Yang, A. Ajmera, R. Knoefler, Y.-W. Teh, F. Jamin, J.E. Park, K. Hooper, C. Griffin, P. Nguyen, V. Klee, V. Ku, C. Baiocco, G. Johnson, L. Tai, J. Benedict, S. Scheer, H. Zhuang, V. Ramanchandran, G. Matusiewicz, Y.-H. Lin, Y.K. Siew, F. Zhang, L.S. Leong, S.L. Liew, K.C. Park, K.-W. Lee, D.H. Hong, S.-M. Choi, E. Kaltalioglu, S.O. Kim, M. Naujok, M. Sherony, A. Cowley, A. Thomas, J. Sudijohno, T. Schiml, J.-H. Ku, I. Yang, 65 nm CMOS technology for low power applications, in *Technical Digest of International Electron Devices Meeting, IEDM*, December 2005, pp. 64–67
 12. F. Arnaud, B. Duriez, B. Tavel, L. Pain, J. Todeschini, M. Jurdit, Y. Laplanche, F. Boeuf, F. Salvetti, D. Lenoble, J.P. Reynard, F. Wacquant, P. Morin, N. Emonet, D. Barge, M. Bidaud, D. Ceccarelli, P. Vannier, Y. Loquet, H. Leninger, F. Judong, C. Perrot, I. Guilmeau, R. Palla, A. Beverina, V. DeJonghe, M. Broekaart, V. Vachellerie, R.A. Bianchi, B. Borot, T. Devoivre, N. Bicaïs, D. Roy, M. Denais, K. Rochereau, R. Difrenza, N. Planes, H. Brut, L. Vishnobulta, D. Reber, P. Stolk, M. Woo, Low cost 65 nm CMOS platform for low power & general purpose applications, in *Symposium on VLSI Technology, Digest of Technical Papers*, June 2004, pp. 10–11
 13. M. Iwai, A. Oishi, T. Sanuki, Y. Takegawa, T. Komoda, Y. Morimasa, K. Ishimaru, M. Takayanagi, K. Eguchi, D. Matsushita, K. Muraoka, K. Sunouchi, T. Noguchi, 45 nm CMOS platform technology (CMOS6) with high density embedded memories, in *Symposium on VLSI Technology, Digest of Technical Papers*, June 2004, pp. 12–13
 14. F. Boeuf, F. Arnaud, M.T. Basso, D. Sotta, F. Wacquant, J. Rosa, N. Bicaïs-Lepinay, H. Bernard, J. Bustos, S. Manakli, M. Gaillardin, J. Grant, T. Skotnicki, B. Tavel, B. Duriez, M. Bidaud, P. Gouraud, C. Chaton, P. Morin, J. Todeschini, M. Jurdit, L. Pain, V. De-Jonghe, R. El-Farhane, S. Jullian, A conventional 45 nm CMOS node low-cost platform for general purpose and low power applications, in *Technical Digest of IEEE International Electron Devices Meeting, IEDM*, December 2004, pp. 425–428
 15. V. Misra, G. Lucovsky, G. Parsons, Issues in high-k gate stack interfaces. *MRS Bull.* **27**, 212–216 (2001)
 16. H.R. Huff, A. Hou, C. Lim, Y. Kim, J. Barnett, G. Bersuker, G.A. Brown, C.D. Young, P.M. Zeitzoff, J. Gutt, P. Lysaght, M.I. Gardner, R.W. Murto, High-k gate stacks for planar, scaled CMOS integrated circuits. *Microelectron. Eng.* **69**, 152–167 (2003)
 17. C. Hobbs, L. Fonseca, V. Dhandapani, S. Samavedam, B. Taylor, J. Grant, L. Dip, D. Triyoso, R. Hegde, D. Gilmer, R. Garcia, D. Roan, L. Lovejoy, R. Rai, L. Hebert, H. Tseng, B. White, P. Tobin, Fermi level pinning at the poly-Si/metal oxide interface, in *Symposium on VLSI Technology, Digest of Technical Papers*, June 2003, pp. 9–10
 18. R. Chau, S. Datta, M. Doczy, B. Doyle, J. Kavalieros, M. Metz, High-k/metal-gate stack and its MOSFET characteristics. *IEEE Electron Device Lett.* **25**(6), 408–410 (2004)
 19. Q. Lu, Y. Yeo, P. Ranade, H. Takeuchi, T. King, Ch. Hu, S.C. Song, H.F. Luan, D. Kwong, Dual-metal gate technology for deep-submicron CMOS transistors, in *Symposium on VLSI Technology, Digest of Technical Papers* (2000), pp. 72–73
 20. K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, C.-H. Choi, G. Ding, K. Fischer, T. Ghani, R. Grover, W. Han, D. Hanken, M. Hattendorf, J. He, J. Hicks, R. Huessner, D. Ingerly, P. Jain, R. James, L. Jong, S. Joshi, C. Kenyon, K. Kuhn, K. Lee, H. Liu, J. Maiz, B. McIntyre, P. Moon, J. Neiryneck, S. Pae, C. Parker, D. Parsons, C. Prasad, L. Pipes, M. Prince, P. Ranade, T. Reynolds, J. Sandford, L. Shifren, J. Sebastian, J. Seiple, D. Simon, S. Sivakumar, P. Smith, C. Thomas, T. Troeger, P. Vandervoorn, S. Williams, K. Zawadzki, A 45 nm logic technology with high-k+metal gate transistors, strained silicon, 9 Cu interconnect layers, 193 nm dry patterning, and 100% Pb-free packaging, in *Technical Digest of International Electron Devices Meeting, IEDM*, December 2007, pp. 247–250

21. T. Skotnicki, G. Merckel, T. Pedron, The voltage-doping transformation: a new approach to the modeling of MOSFET short-channel effects. *IEEE Electron Device Lett.* **9**(3), 109–112 (1988)
22. T. Skotnicki, Heading for decananometer CMOS—is navigation among icebergs still a viable strategy? in *Proceedings of the 30th European Solid-State Device Research Conference, ESSDERC*, September 2000, pp. 19–33
23. J.L. Pelloie, A.J. Auberton-Herv, C. Raynaud, O. Faynot, SOI technology performance and modelling, in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers* (1999), pp. 428–429
24. T. Sekigawa, Y. Hayashi, Calculated threshold-voltage characteristics of an XMOS transistor having an additional bottom gate. *Solid-State Electron.* **27**, 827–828 (1984)
25. J.P. Denton, G.W. Neudeck, Fully depleted dual-gated thin-film SOI P-MOSFETs fabricated in SOI islands with an isolated buried polysilicon backgate. *IEEE Electron Device Lett.* **17**(11), 509–511 (1996)
26. D. Hisamoto, T. Kaga, Y. Kawamoto, E. Takeda, A fully depleted lean-channel transistor (DELTA)-a novel vertical ultra thin SOI MOSFET, in *Technical Digest of International Electron Devices Meeting, IEDM*, December 1989, pp. 833–836
27. D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, C. Hu, FinFET-a self-aligned double-gate MOSFET scalable to 20 nm. *IEEE Trans. Electron Devices* **47**(12), 2320–2325 (2000)
28. B. Doyle, B. Boyanov, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, R. Rios, R. Chau, Tri-gate fully-depleted CMOS transistors: fabrication, design and layout, in *Symposium on VLSI Technology, Digest of Technical Papers*, June 2003, pp. 133–134
29. J.-T. Park, J.-P. Colinge, C.H. Diaz, Pi-gate SOI MOSFET. *IEEE Electron Device Lett.* **22**(8), 405–406 (2001)
30. F.-L. Yang, H.-Y. Chen, F.-C. Chen, C.-C. Huang, C.-Y. Chang, H.-K. Chiu, C.-C. Lee, C.-C. Chen, H.-T. Huang, C.-J. Chen, H.-J. Tao, Y.-C. Yeo, M.-S. Liang, C. Hu, 25 nm CMOS Omega FETs, in *Technical Digest of International Electron Devices Meeting, IEDM* (2002), pp. 255–258
31. J.P. Colinge, *FinFETs and Other Multi-Gate Transistors* (Springer, Berlin, 2008)
32. S.-H. Oh, D. Monroe, J.M. Hergenrother, Analytic description of short-channel effects in fully-depleted double-gate and cylindrical, surrounding-gate MOSFETs. *IEEE Electron Device Lett.* **21**(9), 445–447 (2000)
33. International Technology Roadmap for Semiconductors, <http://www.itrs.net>, 2007 edn. Chap. Emerging Research Devices
34. W. Fischer, Field induced tunnel diode. *IBM Tech. Dis. Bull.* **16**(7), 2303 (1973)
35. P.-F. Wang, Th. Nirschl, D. Schmitt-Landsiedel, W. Hansch, Simulation of the Esaki-tunneling FET. *Solid State Electron.* **47**, 1187–1192 (2003)
36. W.M. Reddick, G.A.J. Amaratunga, Silicon surface tunnel transistor. *Appl. Phys. Lett.* **67**(4), 494–496 (1995)
37. W. Hansch, C. Fink, J. Schulze, I. Eisele, A vertical MOS-gated Esaki tunneling transistor in silicon. *Thin Solid Films* **369**, 387–389 (2000)
38. P. Kinget, M. Steyaert, Impact of transistor mismatch on the speed-accuracy-power trade-off of analog CMOS circuits, in *Proceedings of the IEEE Custom Integrated Circuits Conference, CICC 1996* (1996), pp. 333–336
39. P. Gray, P. Hurst, S. Lewis, R. Meyer, *Analysis and Design of Analog Integrated Circuits*, 4th edn. (Wiley, New York, 2001)
40. P. Wambacq, W. Sansen, *Distortion Analysis of Analog Integrated Circuits* (Kluwer Academic, Dordrecht, 1998)
41. J.A. Croon, M. Rosmeulen, S. Decoutere, W. Sansen, H.E. Maes, An easy-to-use mismatch model for the MOS transistor. *IEEE J. Solid-State Circuits* **37**(8), 1056–1064 (2002)
42. M.J.M. Pelgrom, A.C.J. Duinmaijer, A.P.G. Welbers, Matching properties of MOS transistors. *IEEE J. Solid-State Circuits* **24**(5), 1433–1439 (1989)
43. J.A. Croon, W. Sansen, H.E. Maes, *Matching Properties of Deep Sub-Micron MOS Transistors* (Springer, Berlin, 2005)

44. S. Decoutere, P. Wambacq, V. Subramanian, J. Borremans, A. Mercha, Technologies for (sub-) 45 nm analog/RF CMOS—circuit design opportunities and challenges, in *Proceedings of IEEE Custom Integrated Circuits, CICC* (2006), pp. 679–686
45. B. Razavi, *Design of Analog CMOS Integrated Circuits* (McGraw Hill, New York, 2001)
46. Y. Yausda, T.J. King Liu, C. Hu, Flicker-noise impact on scaling of mixed-signal CMOS with HfSiON. *IEEE Trans. Electron Devices* **55**(1), 417–422 (2008)
47. Z.M. Rittersma, M. Vertregt, W. Deweerdt, S. van Elshocht, P. Srinivasan, E. Simoen, Characterization of mixed-signal properties of MOSFETs with high-k (SiON/HfSiON/TaN) gate stacks. *IEEE Trans. Electron Devices* **53**(5), 1216–1225 (2006)
48. T.L. Tewksbury, H.-S. Lee, Characterization, modeling, and minimization of transient threshold voltage shifts in MOSFETs. *IEEE J. Solid-State Circuits* **29**(3), 239–252 (1994)
49. A. Shanware, M.R. Visokay, J.J. Chambers, A.L.P. Rotondaro, J. McPherson, L. Colombo, Characterization and comparison of the charge trapping in HfSiON and HfO₂ gate dielectrics, in *Technical Digest of International Electron Devices Meeting, IEDM* (2003), pp. 38.6.1–38.6.4
50. M. Fulde, D. Schmitt-Landsiedel, G. Knoblinger, Transient variations in emerging SOI technologies: modeling and impact on analog/mixed-signal circuits, in *Proceedings of IEEE International Symposium on Circuits and Systems, ISCAS* (2006)
51. P. Cuevas, A simple explanation for the apparent relaxation effect associated with hot-carrier phenomenon in MOSFETs. *IEEE Electron Device Lett.* **9**, 627–629 (1988)
52. L.J. McDaid, S. Hall, P.H. Mellor, W. Eccleston, Physical origin of negative differential resistance in SOI transistors. *Electronics Lett.* **25**, 827–828 (1989)
53. J. Jomaah, G. Ghibaudo, F. Balestra, J.L. Pelloie, Impact of self-heating effects on the design of SOI devices versus temperature, in *IEEE International SOI Conference Proceedings* (1995), pp. 114–115
54. N. Collaert, K. von Arnim, R. Rooyackers, T. Vandeweyer, A. Mercha, B. Parvais, L. Witters, A. Nackaerts, E. Altamirano Sanchez, M. Demand, A. Hikavy, S. Demuyne, K. Devriendt, F. Bauer, I. Ferain, A. Veloso, K. De Meyer, S. Biesemans, M. Jurczak, Low-voltage 6T FinFET SRAM cell with high SNM using HfSiON/TiN gate stack, fin widths down to 10 nm and 30 nm gate length, in *Proc. of ICICDT* (2008)
55. A. Veloso, T. Hoffmann, A. Lauwers, H. Yu, S. Severi, E. Augendre, S. Kubicek, P. Verheyen, N. Collaert, P. Absil, M. Jurczak, S. Biesemans, Advanced CMOS device technologies for 45 nm node and below. *Sci. Technol. Adv. Mater.* **8**(3), 214–218 (2007)
56. G. Eneman, M. Jurczak, P. Verheyen, T. Hoffmann, A. De Keersgieter, K. De Meyer, Scalability of strained nitride capping layers for future CMOS generations, in *Proceedings of the 35th European Solid-State Device Research Conference, ESSDERC* (2005), pp. 449–452
57. R. Rooyackers, E. Augendre, B. Degroote, N. Collaert, A. Nackaerts, A. Dixit, T. Vandeweyer, B. Pawlak, M. Ercken, E. Kunnen, G. Dilliway, F. Leys, R. Loo, M. Jurczak, S. Biesemans, Doubling or quadrupling MuGFET fin integration scheme with higher pattern fidelity, lower CD variation and higher layout efficiency, in *Technical Digest of International Electron Devices Meeting, IEDM* (2006), pp. 1–4
58. C.H. Diaz, K. Goto, Y. Yasuda, C. Tsao, T. Chu, W. Lu, V. Chang, Y.T. Hou, Y.S. Chao, P.F. Hsu, C. Chen, K. Lin, J. Ng, W. Yang, C.H. Chen, Y.H. Peng, C.J. Chen, C.C. Chen, M. Yu, L.Y. Yeh, K.S. You, K.S. Chen, K.B. Thei, C.H. Lee, S.H. Yang, J.Y. Cheng, K.T. Huang, J.J. Liaw, Y. Ku, S.M. Jang, H. Chuang, M.S. Liang, 32 nm gate-first high-k/metal-gate technology for high performance low power applications, in *Technical Digest of IEEE International Electron Devices Meeting, IEDM* (2008), pp. 629–632
59. A. Dixit, A. Kottantharayil, N. Collaert, M. Goodwin, M. Jurczak, K. De Meyer, Analysis of parasitic S/D resistance in multiple-gate FETs. *IEEE Trans. Electron Devices* **52**(6), 1132–1140 (2005)
60. M. Guillorn, J. Chang, A. Bryant, N. Fuller, O. Dokumaci, X. Wang, J. Newbury, K. Babich, J. Ott, B. Haran, R. Yu, C. Lavoie, D. Klaus, Y. Zhang, E. Sikorski, W. Graham, B. To, M. Lofaro, J. Tornello, D. Koli, B. Yang, A. Pyzyna, D. Neumeyer, M. Khater, A. Yagishita, H. Kawasaki, W. Haensch, FinFET performance advantage at 22 nm: an AC perspective, in *Symposium on VLSI Technology, Digest of Technical Papers* (2008), pp. 12–13

61. K.R. Laker, W. Sansen, *Design of Analog Integrated Circuits and Systems* (McGraw Hill, New York, 1994)
62. P.E. Allen, D.R. Holberg, *CMOS Analog Circuit Design* (Oxford University Press, London, 2002)
63. V. Subramanian, B. Parvais, J. Borremans, A. Mercha, D. Linten, P. Wambacq, J. Loo, M. Dehan, N. Collaert, S. Kubicek, R.J.P. Lander, J.C. Hooker, S. Donnay, M. Jurczak, G. Groeseneken, W. Sansen, S. Decoutere, Device and circuit-level analog performance trade-offs: a comparative study of planar bulk FETs versus FinFETs, in *Technical Digest of International Electron Devices Meeting, IEDM* (2005), pp. 898–901
64. A. Chatterjee, K. Vasanth, D.T. Grider, M. Nandakumar, G. Pollak, R. Aggarwal, M. Rodder, H. Shichijo, Transistor design issues in integrating analog functions with high performance digital CMOS, in *Symposium on VLSI Technology, Digest of Technical Papers* (1999), pp. 147–148
65. B. Min, S.P. Devireddy, Z. Celik-Butler, W. Fang, A. Zlotnicka, H. Tseng, P. Tobin, Low frequency noise in submicrometer MOSFETs with HfO₂, HfO₂/Al₂O₃ and HfAlO_x gate stacks. *IEEE Trans. Electron Devices* **51**(10), 1679–1687 (2004)
66. M. Fulde, A. Mercha, C. Gustin, B. Parvais, V. Subramanian, K. von Arnim, F. Bauer, K. Schrufer, G. Knoblinger, D. Schmitt-Landsiedel, Analog design challenges and trade-offs using emerging materials and devices, in *Proceedings of 33th European Solid-State Circuits Conference, ESSCIRC*, September 2007, pp. 123–126
67. X. Chen, S. Samavedam, V. Narayanan, K. Stein, C. Hobbs, C. Baiocco, W. Li, D. Jaeger, M. Zaleski, H. Yang, N. Kim, Y. Lee, D. Zhang, L. Kang, J. Chen, H. Zhuang, A. Sheik, J. Wallner, M. Aquilino, J. Han, Z. Jin, J. Li, G. Massey, S. Kalpat, R. Jha, N. Moumen, R. Mo, S. Kirshnan, X. Wang, M. Chudzik, M. Chowdhury, D. Nair, C. Reddy, Y.-W. Teh, C. Kothandaraman, D. Coolbaugh, S. Pandey, D. Tekleab, A. Thean, M. Sherony, C. Lage, J. Sudijohno, R. Lindsay, J.-H. Ku, M. Khare, A. Steegen, A cost effective 32 nm high-k/metal gate CMOS technology for low power applications with single-metal/gate-first process, in *Symposium on VLSI Technology, Digest of Technical Papers* (2008), pp. 88–89
68. M. Sato, Y. Sugita, T. Aoyama, Y. Nara, Y. Ohji, Impact of different nature of interface defect states on the NBTI and 1/f noise of high-k/metal-gate pMOSFETs between (100) and (110) crystal orientation, in *Symposium on VLSI Technology, Digest of Technical Papers* (2008), pp. 64–65
69. International Technology Roadmap for Semiconductors, <http://www.itrs.net>, 2007 edn. Chap. Radio Frequency and Analog/Mixed-Signal Technologies for Wireless Communications
70. T. Schulz, W. Xiong, C.R. Cleavelin, K. Schrufer, M. Gostkowski, K. Matthews, G. Gebara, R.J. Zaman, P. Patruno, A. Chaudhry, A. Woo, J.P. Colinge, Fin thickness asymmetry effects in multiple-gate SOI FETs (MuGFETs), in *Proceedings of the IEEE International SOI Conference* (2005), pp. 154–156
71. C. Gustin, A. Mercha, J. Loo, V. Subramanian, B. Parvais, M. Dehan, S. Decoutere, Stochastic matching properties of FinFETs. *IEEE Electron Device Lett.* **27**(10), 846–848 (2006)
72. M. Fulde, F. Kuttner, K. von Arnim, B. Parvais, A. Mercha, N. Collaert, R. Rooyackers, D. Schmitt-Landsiedel, G. Knoblinger, A 10-bit current-steering FinFET D/A converter, in *IEEE International SOI Conference Proceedings*, October 2008, pp. 95–96
73. H. Reisinger, O. Blank, W. Heinrigs, A. Muhlhoff, W. Gustin, C. Schlunder, Analysis of NBTI degradation- and recovery-behavior based on ultra fast VT-measurements, in *Reliability Physics Symposium Proceedings, 2006. 44th Annual., IEEE International* (2006), pp. 448–453
74. S. Pae, M. Agostinelli, M. Brazier, R. Chau, G. Dewey, T. Ghani, M. Hattendorf, J. Hicks, J. Kavalieros, K. Kuhn, M. Kuhn, J. Maiz, M. Metz, K. Mistry, C. Prasad, S. Ramey, A. Roskowski, J. Sandford, C. Thomas, J. Thomas, C. Wiegand, J. Wiedemer, BTI reliability of 45 nm high-K + metal-gate process technology, in *Proceedings of 46th Annual International Reliability Physics Symposium, Phoenix* (2008), pp. 352–357
75. B.M. Tenbroek, M.S.L. Lee, W. Redman-White, R.J.T. Bunyan, M.J. Uren, Impact of self-heating and thermal coupling on analog circuits in SOI CMOS. *IEEE J. Solid-State Circuits* **33**(7), 1037–1046 (1998)

76. W. Molzer et al., Self heating simulation of multi-gate FETs, in *Proceedings of 36th European Solid-State Device Research Conference, ESSDERC* (2006), pp. 311–314
77. B.M. Tenbroek, M.S.L. Lee, W. Redman-White, R.J.T. Bunyan, M.J. Uren, Self-heating effects in SOI MOSFETs and their measurement by small signal conductance techniques. *IEEE Trans. Electron Devices* **43**(12), 2240–2249 (1996)
78. L. Bertolissi, Modeling and simulation of self-heating effects in deep sub-micron silicon on insulator (SOI) technologies for analog circuits. M.Sc. Thesis, Universita Degli Studi di Udine (2004)
79. B. Razavi, *RF Microelectronics* (Prentice Hall, New York, 1998)
80. T.L. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits* (Cambridge University Press, Cambridge, 2004)
81. A. Hajimiri, T.H. Lee, A general theory of phase noise in electrical oscillators. *IEEE J. Solid State Circuits* **33**(2), 179–194 (1998)
82. K.C. Hsieh, P. Gray, D. Senderowicz, D.G. Messerschmitt, A low-noise chopper-stabilized switched capacitor filtering technique. *IEEE J. Solid State Circuits* **16**(6), 708–715 (1981)
83. R. Gregorian, G.C. Temes, *Analog MOS Integrated Circuits for Signal Processing* (Wiley, New York, 1986)
84. I. Bloom, Y. Nemirovsky, $1/f$ noise reduction of metal-oxide-semiconductor transistors by cycling from inversion to accumulation. *Appl. Phys. Lett.* **58**(15), 1664–1666 (1991)
85. E.A.M. Klumperink, S.L.J. Gierkink, A.P. van der Wel, B. Nauta, Reducing MOSFET $1/f$ noise and power consumption by switched biasing. *IEEE J. Solid State Circuits* **35**(7), 994–1001 (2000)
86. J. Koh, R. Thewes, D. Schmitt-Landsiedel, R. Brederlow, A circuit design-based approach for $1/f$ -noise reduction in linear analog CMOS ICs, in *Symposium on VLSI Technology, Digest of Technical Papers* (2004), pp. 222–225
87. J. Koh, D. Schmitt-Landsiedel, R. Thewes, R. Brederlow, A complementary switched MOSFET architecture for the $1/f$ noise reduction in linear analog CMOS ICs. *IEEE J. Solid State Circuits* **42**(6), 1352–1361 (2007)
88. D. Siprak, N. Zanolta, M. Tiebout, P. Baumgartner, C. Fiegna, Reduction of low-frequency noise in MOSFETs under switched gate and substrate bias, in *Proceedings of the 38th European Solid-State Device Research Conference, ESSDERC* (2008), pp. 266–269
89. D. Siprak, M. Tiebout, P. Baumgartner, Reduction of VCO phase noise through forward substrate biasing of switched MOSFETs, in *Proceedings of 34th European Solid State Conference, ESSCIRC* (2008), pp. 326–329
90. M. Ertuerk, T. Xia, W. Clark, Gate voltage dependence of MOSFET $1/f$ noise statistics. *IEEE Electron Device Lett.* **28**(9), 812–814 (2007)
91. B. Razavi, *Principles of Data Conversion System Design* (IEEE Press, New York, 1995)
92. F. Kuttner, A 1.2 V 10b 20MSample/s non-binary successive approximation ADC in 0.13 μm CMOS, in *IEEE International Solid-State Circuits Conference, Digest of Technical Papers*, vol. 1 (2002), pp. 176–177
93. R. Schreier, G.C. Temes, *Understanding Delta-Sigma Data Converters* (Wiley, New York, 2004)
94. S.R. Norsworthy, R. Schreier, G.C. Temes, *Delta-SIGMA Data Converters: Theory, Design, and Simulation* (IEEE Press, New York, 1996)
95. G.D.J. Smit, A.J. Scholten, N. Serra, R.M.T. Pijper, R. van Langevelde, A. Mercha, G. Goldenblatt, D.B.M. Klaassen, PSP-based compact FinFET model describing DC and RF measurements, in *Technical Digest of International Electron Devices Meeting, IEDM*, December 2006, pp. 1–4
96. W. Sansen, *Analog Design Essentials* (Springer, Berlin, 2006)
97. K.E. Kuijk, A precision reference voltage source. *IEEE J. Solid State Circuits* **SC-8**, 222–226 (1973)
98. S.M. Sze, *Physics of Semiconductor Devices* (Wiley, New York, 1981)
99. U. Feldmann, Diode model in TITAN V006. Technical Report, Infineon Technologies, TITAN group (2005)

100. M. Wirnshofer, Evaluation of voltage reference circuits using novel devices. M.S. Thesis, Technische Universität München (2007)
101. H. Banba, H. Shiga, A. Umezawa, T. Miyaba, T. Tanzawa, S. Atsumi, K. Sakui, A CMOS bandgap reference circuit with sub-1-V operation. *IEEE J. Solid State Circuits* **34**(5), 670–674 (1999)
102. M. Fulde, M. Wirnshofer, G. Knoblinger, D. Schmitt-Landsiedel, Design of low-voltage bandgap reference circuits in multi-gate CMOS technologies, in *Proceedings of IEEE International Symposium on Circuits and Systems, ISCAS* (2009), pp. 234–237
103. J.A. Schoeff, An inherently monotonic 12 bit DAC. *IEEE J. Solid-State Circuits* **14**, 904–911 (1979)
104. A. van den Bosch, M.A.F. Borremans, M.S.J. Steyaert, W. Sansen, A 10-bit 1-GSample/s Nyquist current-steering CMOS D/A converter. *IEEE J. Solid-State Circuits* **36**(3), 315–324 (2001)
105. A. van den Bosch, M. Steyaert, W. Sansen, SFDR-bandwidth limitations for high speed high resolution current steering CMOS D/A converters, in *Proceedings of the IEEE International Conference on Electronics, Circuits and Systems, ICECS*, vol. 3 (1999), pp. 1193–1196
106. A. Van den Bosch, M. Steyaert, W. Sansen, An accurate statistical yield model for CMOS current-steering D/A converters, in *Proceedings of IEEE International Symposium on Circuits and Systems, ISCAS*, vol. 4 (2000), pp. 105–108
107. W.-S. Chou, S.-C. Yang, F.-L. Hsueh, H.-C. Huang, C.-J. Hsiao, A low-cost triple-channel 10-bit 250 MHz DAC IP in 65 nm CMOS process, in *Proceedings of IEEE International Symposium on Circuits and Systems, ISCAS* (2007), pp. 3594–3597
108. D.C. Lee, Analysis of jitter in phase-locked loops. *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.* **49**(11), 704–711 (2002)
109. B. Razavi, *Monolithic Phase-Locked Loops and Clock Recovery Circuits* (IEEE Press, New York, 1996)
110. S. Williams, H. Thompson, M. Hufford, E. Naviasik, An improved CMOS ring oscillator PLL with less than 4 ps RMS accumulated jitter, in *Proceedings of IEEE Custom Integrated Circuits Conference* (2004), pp. 151–154
111. H. Arora, N. Klemmer, J.C. Morizio, P.D. Wolf, Enhanced phase noise modeling of fractional-N frequency synthesizers. *IEEE Trans. Circuits Syst. I Regul. Pap.* **52**(5), 379–395 (2005)
112. Z. Cao, Y. Li, S. Yan, A 0.4 ps-RMS-jitter 1–3 GHz ring-oscillator PLL using phase-noise preamplification. *IEEE J. Solid State Circuits* **43**(9), 2079–2089 (2008)
113. N. DaDalt, C. Sandner, Private communication
114. R. Nonis, Phase noise modelling in phase lock loop frequency synthesizers. M.S. Thesis, University of Udine (2002)
115. L. Bizjak, N. DaDalt, P. Thurner, R. Nonis, P. Palestri, L. Selmi, Comprehensive behavioral modeling of conventional and dual-tuning PLLs. *IEEE Trans. Circuits Syst. I Regul. Pap.* **55**, 1628–1638 (2008)
116. A. Hajimiri, S. Limotyrakis, T.H. Lee, Jitter and phase noise in ring oscillators. *IEEE J. Solid State Circuits* **34**(6), 790–804 (1999)
117. G. Knoblinger, M. Fulde, D. Siprak, U. Hodel, K. von Arnim, T. Schulz, C. Pacha, U. Baumann, W. Marshall, A. Xiong, C.R. Cleavelin, P. Patruno, K. Schroefer, Evaluation of FinFET RF building blocks, in *IEEE International SOI Conference Proceedings*, October 2007, pp. 39–40
118. M. Fulde, K. von Arnim, C. Pacha, F. Bauer, C. Russ, D. Siprak, W. Xiong, A. Marshall, C.R. Cleavelin, K. Schroefer, D. Schmitt-Landsiedel, G. Knoblinger, Advances in multi-gate MOSFET circuit design, in *Proceedings of the 14th IEEE International Conference on Electronics, Circuits and Systems, ICECS*, December 2007, pp. 186–189
119. M. Tiebout, *Low Power VCO Design in CMOS* (Springer, Berlin, 2005)
120. M. Dehan, B. Parvais, V. Subramanian, C. Gustin, J. Loo, A. Mercha, S. Decoutere, Characterization, modeling, and optimization of FinFET MOS varactors, in *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems* (2007), pp. 28–31

121. J. Janssens, M. Steyaert, H. Miyakawa, A 2.7 V CMOS broadband low noise amplifier, in *Symposium on VLSI Circuits, Digest of Technical Papers* (1997), pp. 87–88
122. M. Tiebout, E. Paporisto, LNA design for a fully integrated CMOS single chip UMTS transceiver, in *Proceedings of the 28th European Solid-State Circuits Conference, ESSCIRC* (2002), pp. 835–838
123. B. Parvais, C. Gustin, V. de Heyn, J. Loo, M. Dehan, V. Subramanian, A. Mercha, N. Collaert, R. Rooyackers, M. Jurczak, P. Wambacq, S. Decoutere, Suitability of FinFET technology for low-power mixed-signal applications, in *IEEE International Conference on Integrated Circuit Design and Technology, ICICDT'06* (2006), pp. 1–4
124. P. Wambacq, B. Verbruggen, K. Scheir, J. Borremans, V. De Heyn, G. Van der Plas, K. Mercha, Bb. Parvais, V. Subramanian, M. Jurczak, S. Decoutere, S. Donnay, Analog and RF circuits in 45 nm CMOS and below: planar bulk versus FinFET, in *Proceedings of 33rd European Solid State Conference, ESSCIRC* (2006), pp. 54–57
125. B.M. Tenbroek, W. Redman-White, M.S.L. Lee, R.J.T. Bunyan, M.J. Uren, K.M. Brunson, Characterization of layout dependent thermal coupling in SOI CMOS current mirrors. *IEEE Trans. Electron Devices* **43**(12), 2227–2232 (1996)
126. I.M. Filanovsky, A. Allam, Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits. *IEEE Trans. Circuits Syst. I Fundam. Theory Appl.* **48**, 876–884 (2001)
127. M. Fulde, J.P. Engelstaedter, G. Knoblinger, D. Schmitt-Landsiedel, Analog circuits using FinFETs: benefits in speed-accuracy-power trade-off and simulation of parasitic effects. *Adv. Radio Sci. Kleinheubacher Berichte* 2006 **5**, 285–290 (2007)
128. V. Subramanian, A. Mercha, B. Parvais, J. Loo, C. Gustin, N. Collaert, M. Jurczak, G. Groeseneken, W. Sansen, S. Decoutere, Optimization of FinFET geometries for analog performance, in *Proceedings of ULIS* (2006)
129. C. Kienmayer, An integrated 17 GHz receiver in 0.13 um CMOS for wireless applications. Ph.D. Thesis, Technische Universität Wien (2004)
130. A. Bargagli-Stoffi, *Ultra Low-Voltage, Low-Power Amplifiers in Deep-Submicrometer CMOS* (Shaker, Maastricht, 2006)
131. T. Nirschl, *Circuit Applications of the Tunneling Field Effect Transistor (TFET)* (Shaker, Maastricht, 2008)
132. M. Fulde, A. Heigl, M. Weis, M. Wirmshofer, K.V. Arnim, T. Nirschl, M. Sterkel, G. Knoblinger, W. Hansch, G. Wachutka, D. Schmitt-Landsiedel, Fabrication, optimization and application of complementary multiple-gate tunneling FETs, in *Proceedings of 2nd IEEE International Nanoelectronics Conference*, March 2008, pp. 946–951
133. Q. Zhang, W. Zhao, A. Seabaugh, Low-subthreshold-swing tunnel transistors. *IEEE Electron Device Lett.* **27**(4), 297–300 (2006)
134. K. Boucart, A. Ionescu, Threshold voltage in tunnel FETs: physical definition, extraction, scaling and impact on IC design, in *Proceedings of the 37th European Solid-State Device Research Conference, ESSDERC* (2007), pp. 299–302
135. G.A.M. Hurkx, D.B.M. Klaassen, M.P.G. Knuvers, A new recombination model for device simulation including tunneling. *IEEE Trans. Electron Devices* **39**, 331–338 (1992)
136. T. Nirschl, P.-F. Wang, W. Hansch, D. Schmitt-Landsiedel, The tunneling field effect transistors (TFET): the temperature dependence, the simulation model, and its application, in *Proceedings of the International Symposium on Circuits and Systems, ISCAS*, vol. 3 (2004), pp. 713–716
137. M. Fulde, A. Wachutka, G. Heigl, D. Schmitt-Landsiedel, Complementary multi-gate tunneling FETs: fabrication, optimization and application aspects. *Int. J. Nanotechnology* **6**(7/8), 628–639 (2009)
138. A. Heigl, G. Wachutka, Simulation of advanced tunneling devices, in *International Conference on Advanced Semiconductor Devices and Microsystems, ASDAM* (2006), pp. 121–124

139. A. Heigl, G. Wachutka, Optimization of vertical tunneling field-effect transistors, in *Proc. of ULIS (2007)*, pp. 133–136
140. W.Y. Choi, J.Y. Song, J.D. Lee, Y.J. Park, B.-G. Park, 70-nm impact-ionization metal-oxide-semiconductor (I-MOS) devices integrated with tunneling field-effect transistors (TFETs), in *Technical Digest of International Electron Devices Meeting, IEDM (2005)*, pp. 955–958