Models in Hardware Testing

FRONTIERS IN ELECTRONIC TESTING

Consulting Editor
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Volume 43

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Hans-Joachim Wunderlich
Editor

Models in Hardware Testing

Lecture Notes of the Forum in Honor of Christian Landrault

Springer

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ISSN 0929-1296
ISBN 978-90-481-3281-2 e-ISBN 978-90-481-3282-9
DOI 10.1007/978-90-481-3282-9
Springer Dordrecht Heidelberg London New York

Library of Congress Control Number: 2009939835

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Cover design: eStudio Calamar S.L.

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

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Preface

Model based testing is one of the most powerful techniques for testing hardware and software systems. While moving forward to nanoscaled CMOS circuits, we observe a plethora of new defect mechanisms, which require increasing efforts in systematic fault modeling and appropriate algorithms for test generation, fault simulation and diagnosis. The text presented here treats models and especially fault models in hardware testing in a comprehensive way, considers the most recent state of the art and puts them into their historical context.

The first chapter by Joan Figueras et al. considers the fact that open defects are becoming the predominant failure mechanism as technologies are scaled down. It analyzes these defects according to their locations and resistive nature, and deduces the faulty behavior. This chapter lays foundations for the subsequently described algorithms and proposes test strategies to improve the detectability and diagnosability of open defects.

The second large class of defects is formed by bridges and treated in chapter 2 by M. Renovell et al. Bridging defects are also responsible for a large percentage of failure in CMOS technologies, and their impact in nanometer technologies with dense interconnect structures will increase. The chapter explores the logic detectability of bridging defects by taking into account different ranges of resistances. The concept of an Analog Detectability Interval (ADI) and its use for increasing the quality of test vectors and the fault coverage are introduced.

Both resistive bridges and resistive opens may result in timing faults. Chapter 3 on delay faults by S. Reddy describes methods to generate appropriate tests and design for test methods to improve delay fault coverage. So-called small delay faults are only observable at a subset of paths in the circuit, and they are increasingly relevant in nanoscaled technologies. This chapter treats them as a part of ongoing research.

Two chapters deal with the algorithmic aspects introduced by the complex fault models described so far. Chapter 4 on fault modeling for simulation and test pattern generation by B. Becker and I. Polian presents algorithms which can handle the resistive fault models described above. It covers in detail the abstraction mechanisms required, the algorithms and their optimizations.

Chapter 5 on generalized fault modeling for logic diagnosis by H.-J. Wunderlich and S. Holst deals with the problem that in contrast to ATPG and fault simulation,

diagnosis algorithms should not make pre-assumptions on the appropriate fault model but have to identify the faulty behavior instead. A generalized fault modeling technique and notation are introduced, and diagnosis techniques are proposed which can handle this fault modeling at a higher level of abstraction.

Larger and larger portions of the IC area are occupied by memory, and semiconductor memories have always been used to push silicon technology at its limits. This makes these devices extremely sensitive to physical defects and environmental influences that may severely compromise their correct behavior. Chapter 6 on models in memory testing by S. Di Carlo and P. Prinetto provides an overview of models and notations currently used and highlights challenging problems awaiting solutions.

Chapter 7 by P. Girard and H.-J. Wunderlich introduces power consumption during test as an additional aspect. In test mode, power consumption is even more critical than in system mode, and has severe impact on reliability, yield and test costs. This chapter describes models of different types and sources of test power. Power-aware techniques for test pattern generation, design for test and test data compression are presented which require minimized hardware cost and test application time.

The last chapter by J. Arlat and Y. Crouzet discusses physical fault models and fault tolerance. Dependability, online test and fault tolerance techniques receive more and more attention for nanoscaled devices. This chapter focuses on the representativeness of fault models with respect to physical faults for deriving relevant test procedures and experimental assessment techniques. The chapter links physical fault models to fault injection based dependability assessment techniques.

The authors of this book provided this comprehensive treatment of models in hardware testing in appreciation of the achievements of Christian Landrault who laid the foundations of many of the concepts presented here during his research life, and had a leading role in the European test and research community. The authors of this book are close colleagues and friends of Christian Landrault, and dedicating this book to him is their way to say thank you for many years of friendship and fruitful collaborations.

Sevilla
May 28, 2009

Hans-Joachim Wunderlich

To Christian: a Real Test and Taste Expert

Dear Christian,

Writing and setting up this book has been our way to express our deep and sincere THANKS!! In fact, we all owe you many THANKS for so many things and at so many "levels". Let's try to focus on some of them, starting with the scientific ones.

Your research interests and activities spanned several topics and areas, in each getting significant results and providing original contributions. As evidence of this, one should simply look at all the references to your papers at the end of each chapter of this book. In addition to these very significant "written" contributions, we have to thank you for the "oral" ones: your discussions during the conferences you attended have always been characterized by a constructive approach, always aimed at understanding, helping, and providing hints.

Thanks to all your efforts and to your capability of selecting high quality researchers and co-workers, your team at LIRMM has grown to become one of the highly recognized key players not only at the European level but also in the international test research community!!

The list of scientific events you served as General Chair, Program Chair, Steering Committee member, and Program Committee member is too long to list here and if we try to list we would definitely forget a lot of them.

The scientific community in general and the overall test community in particular owe you a gigantic thank you for the unbelievable amount of time and efforts you spent to serve them.

You have been a father (if not the father) of the European Test Community. Your strength, your dedication, your patience, your leadership, and your efforts allowed the community to grow; from the first presence at the CAVE Workshops to the Design for Testability Workshops, from the European Test Conferences to DATE, from the European Test Workshops to the European Test Symposiums (ETS). Under your leadership, the European Group of the IEEE Test Technology Technical Council grew significantly, becoming one of the most active regional groups of the council.

Your vision led to the creation of the European Test Symposium Steering Committee. Under your chairpersonship, the Committee started playing a key role in assuring to maintain those high quality levels that are unanimously recognized as the hallmark of ETS not only in Europe, but worldwide as well.

Dear Christian, last but definitely not least, we have to thank you at the personal and human level. The so many hours spent together discussing, eating, tasting wine, talking of culture, sharing everyday problems of our private lives, telling us your experiences in fishing and hunting, have been invaluable. It will be very hard for all of us attending next scientific and technical events without your friendliness. We will look for you until we realize that, instead of attending yet another boring panel session, you will be most likely hunting, or fishing, or enjoying Titou, your sons, and your granddaughters… lucky you!!

Amicalement
Your friends of the test community

From LAAS to LIRMM and Beyond

For the contributors to this book, as well as for many researchers in the field of testing and testability of integrated digital circuits and systems, Christian Landrault is one of the key figures in the research, development and teaching of this very important field.

Christian Landrault began his scientific life at LAAS-CNRS in Toulouse where he stayed during 10 years (1970–1980), just after his graduation as an Engineer from the prestigious *Ecole Nationale d'Ingénieurs de Constructions Aéronautiques*.

During this period, he was a member of the "Digital Automatisms" research team that I headed and which was subsequently led by Jean-Claude Laprie, to become the research group on "Dependable Computing and Fault Tolerance" as it is known today. Christian Landrault obtained his Ph.D. (1973) and *Doctorat d'Etat* (1977) at LAAS, both from the National Polytechnic Institute of Toulouse (INPT), respectively on the design of control systems, and on the modeling and evaluation of fault-tolerant computer architectures. Then, by the end of the 1970s, he initiated his pioneering work in the domain of hardware digital technology, in particular on fault modeling and testability of MOS integrated circuits, as well as on the design of self-checking microprocessor chips. This seminal work has resulted in a couple of papers that are among the most referenced papers at LAAS and that form the main basis for a large part of the material reported in Chapter 8 of this book.

In 1980, Christian joined LIRMM in Montpellier, in the Microelectronics Department. The research activities he developed and the related results attained, span mainly the area of testing and testability of digital integrated circuits: fault simulation, ATPG, DFT, BIST and fault tolerance. The results he obtained on these topics were published in more than one hundred papers in leading journals and conferences worldwide. Christian Landrault has always contributed very actively to the discussions and reflections in line with the state-of-the-art, the challenges, the evolution and prospects of the field with his academic and industrial colleagues.

Christian Landrault has been a member of numerous Program Committees of major conferences and workshops in the area of testing, among which, ITC, VTS, ATS, ETS, DATE, etc., which confirms the leading role he has played in the emergence and blooming of the scientific community on testing and testability. In particular, he has been the founder of the European Test Workshop in 1996 for which he was the first Chairman and has subsequently chaired the PC in 1998 and 1999. This

event has since become a Symposium and its 14th edition has taken place this year. Christian was until 2008 the Elected Chair of the Steering Committee of the Symposium. He was also the European representative at the ITC Program Committee for several years.

To conclude, I would like to emphasize that, beyond his well-recognized skills and professional competencies, Christian possesses a rather unique sense for dialogue and friendship, and this is as a friend that I would like to tell him that we are all proud and pleased for the outstanding scientific career he has conducted with his colleagues, both at LAAS and at LIRMM, but also with researchers from the entire world.

Toulouse,
March 16, 2009

Professor Alain Costes
Director of LAAS-CNRS (1984–1996)
Chairman of INPT (1996–2000)
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