Debugging at the Electronic System Level

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Springer

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ISBN 978-90-481-9254-0 e-ISBN 978-90-481-9255-7
DOI 10.1007/978-90-481-9255-7
Springer Dordrecht Heidelberg London New York

Library of Congress Control Number: 2010929863

Cover design: eStudio Calamar S.L.

Printed on acid-free paper

Springer is part of Springer Science+Business Media (www.springer.com)

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Preface

Debugging becomes more and more the bottleneck to chip design productivity, especially while developing modern complex and heterogenous integrated circuits and systems at the *Electronic System Level* (ESL). Today, debugging is still an unsystematic and lengthy process. Here, a simple reporting of a failure is not enough, anymore. Rather, it becomes more and more important not only to find many errors early during development but also to provide efficient methods for their isolation. In this book the state-of-the-art of modeling and verification of ESL designs is reviewed. There, a particular focus is taken onto SystemC. Then, a reasoning hierarchy is introduced. The hierarchy combines well-known debugging techniques with whole new techniques to improve the verification efficiency at ESL. The proposed systematic debugging approach is supported amongst others by static code analysis, debug patterns, dynamic program slicing, design visualization, property generation, and automatic failure isolation. All techniques were empirically evaluated using real-world industrial designs. Summarized, the introduced approach enables a systematic search for errors in ESL designs. Here, the debugging techniques improve and accelerate error detection, observation, and isolation as well as design understanding.

Acknowledgements

We would like to thank all colleagues of Division Design Automation of Fraunhofer Institute for Integrated Circuits in Dresden and all members of the research group for computer architecture in Bremen for the amazing atmosphere during research and work and the many fruitful discussions.

Moreover, we are grateful to all our coauthors of the papers that make up an important part of this book: Thomas Berndt, Erhard Fehlauer, Görschwin Fey, Christian Genz, Christian Haufe, Thomas Klotz, Sebastian Ohnewald, and Steffen Rülke. Additionally, we would like to thank our students who had contributed many prototype implementations: Lars Ehrler, Dirk Linke, Dominic Scharfe, Tom Schiekel, and Richard Wähner.

Erhard Fehlauer, Görschwin Fey, and Steffen Rülke helped us in proofreading and improving the presentation.

FRANK ROGIN AND ROLF DRECHSLER
Bremen, March 2010